REMARKS

Claims 1, 4, 5, 8-18 and 21-28 are pending in this application. By this Amendment, claims 1, 4, 5,14, 17 and 18 are amended. The amendments introduce no new matter. Claims 6, 7, 19 and 20 are canceled without prejudice to, or disclaimer of, the subject matter recited in those claims. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

Applicant appreciates the courtesies shown to Applicant's representative by Examiner Sherman during the December 27, 2007 personal interview. Applicant's separate record of a summary of the substance of the personal interview is contained in the following remarks.

The Office Action, in paragraph 2, maintains the finality of the June 28, 2007 Restriction Requirement between Group I, claims 1, 4, 5, 8-18 and 21-28, drawn to an electronic circuit comprising a first and a second circuit unit and a current mirror; and Group II, claims 6, 7, 19 and 20, drawn to an electronic circuit comprising a single circuit unit. The Office Action withdraws from consideration claims 6, 7, 19 and 20. Without conceding the propriety of this Requirement, claims 6, 7, 19 and 20 are canceled.

The Office Action, in paragraph 4, objects to the drawings under 37 C.F.R. §1.83(a) as allegedly failing to show every feature specified in the claims. In particular, the Office Action asserts that the features of a first circuit unit including a plurality of transistors connected in series and a second circuit unit including a plurality of transistors connected in parallel, as previously recited in claim 5, are not shown in the drawings. During the December 27 personal interview, Applicant's representative argued that Fig. 3 clearly shows a first circuit unit and second circuit unit each with a plurality of transistors and one with transistors connected in series and the other with transistors connected in parallel. The Examiner maintained that the drawings depict only a first circuit unit including a plurality of transistors connected in parallel and not in series and a second circuit unit including a

plurality of transistors connected in series and not in parallel, as recited in claim 5. No agreement was reached.

However, as discussed during the personal interview, even under the Office Action's reading of the pending claims in light of the drawings, Applicant clearly discloses in paragraph [0095] that the transistors in circuit unit 40 can be connected in parallel (as shown in Fig. 3) or in series and the transistors in circuit unit 30 can be connected in series (as shown in Fig. 3) or in parallel. At least because Fig. 3 depicts a circuit unit in parallel (element 40) and another circuit unit in series (element 30), one of ordinary skill in the art would have understood and would have been enabled by the features recited in claim 5 in view of at least the disclosure in paragraph [0095].

The Office Action, in paragraph 5, objects to claims 1 and 14 as being indefinite. Specifically, the Office Action asserts that the feature of each of the at least one of the first circuit unit and the second circuit unit having the plurality of transistors having the same driving capability, as recited previously recited in claims 1 and 14, is unclear. Claims 1 and 14 are amended to obviate this objection.

The Office Action, in paragraph 7, rejects claims 1 and 14 under 35 U.S.C. §112, second paragraph, as being indefinite.

First, the Office Action asserts that claims 1 and 14 are indefinite because these claims recite "a switching element mutually connected to a plurality of transistors in the first circuit unit" and "at least one of the first circuit unit and the second circuit unit includes a plurality of transistors connected in series or in parallel." Claims 1 and 14 are amended to obviate this rejection.

Second, the Office Action asserts that these claims are indefinite for the reasons discussed above with respect to the objection of claims 1 and 14. The amendments to claims 1 and 14 also obviate this rejection.

The Office Action, in paragraph 10, rejects claims 1, 4, 5, 8-14, 17, 18 and 21-28 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,909,242 to Kimura. This rejection is respectfully traversed.

The Office Action, in paragraph 10, asserts that Kimura would have rendered obvious the combinations of all of the features recited in independent claims 1 and 14. The analysis of the Office Action fails for at least the following reasons.

Kimura does not teach, nor can it reasonably be considered to have suggested, respective gates of the plurality of transistors in the first circuit unit being mutually connected to the respective gates of the plurality of transistors in the second circuit unit, as recited in claims 1 and 14. The Office Action, however, fails to even address where Kimura teaches, or would have rendered obvious this feature. During the December 27 personal interview, the Examiner indicated that clarifying the relationship between the first and second circuit unit should overcome the rejections of the Office Action. Claims 1 and 14 are amended to clarify this relationship. For at least these reasons, it is unreasonable to assert that Kimura teaches, or would have rendered obvious, at least this feature.

Kimura also does not teach, nor can it reasonably be considered to have suggested, the plurality of transistors in the first circuit unit and the plurality of transistors in the second circuit unit have the same driving capability, as recited in claims 1 and 14. The Office Action asserts that Kimura discloses in col. 6, lines 62-67 a relationship between TFTs that can be considered to correspond to the feature of each of the at least one of the first circuit unit and the second circuit unit having the plurality of transistors having the same driving capability, as previously recited in claims 1 and 14. Fig. 19 and col. 6, lines 62-67 of Kimura, however, teach that the gate length and the channel width of TFTs 1907 and TFTs 1908 dictate the relationship between the signal electric current and the electric current flowing in the EL element to be equal. Claims 1 and 14 are amended to clarify that it is the plurality of

transistors in the first circuit unit and the plurality of transistors in the second circuit unit that have the same driving capability. It is unreasonable to assert that Kimura teaches at least this feature.

For at least the foregoing reasons, the applied reference cannot reasonably be considered to have suggested the combinations of all of the features positively recited in independent claims 1 and 14. Additionally, claims 4, 5, 8-13, 15-18 and 21-28 also would not have been suggested by the applied reference for at least the respective dependence of these claims on allowable base claims, as well as for the separately patentable subject matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejection of the 1, 4, 5, 8-18 and 21-28 under 35 U.S.C. §103(a) as being unpatentable over the applied reference are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 4, 5, 8-18 and 21-28 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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JAO:CJW/clf

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